

IN THE CLAIMS:

Please cancel claims 4-5, add new claims 35-36, and amend the remaining claims as follows:

1. (Currently Amended) An integrated circuit structure comprising:
 - a substrate;
 - first-type transistors on said substrate, wherein said first-type transistors comprise first gate conductors and first spacers adjacent said first gate conductors;
 - second-type transistors on said substrate, wherein said second-type transistors comprise second gate conductors, said first spacers adjacent said second gate conductors, an etch stop layer on said first spacers, and second spacers on said etch stop layer, wherein said etch stop layer is only on said first spacers that are adjacent said second gate conductors and said etch stop layer is not on said first spacers that are adjacent said first gate conductors;
 - an oxide layer, wherein said oxide layer is on said first gate conductors and said second gate conductors, wherein said first spacers are on said oxide layer, and wherein said etch stop layer is between bottom surfaces of said second spacers and said oxide layer;
 - first silicide regions proximate said first spacers of said first-type transistors; and
 - second silicide regions proximate said second spacers of said second-type transistors, wherein said second silicide regions are farther from said second gate conductors than said first silicide regions are from said first gate conductors;
 - first-type impurity implants in areas of said substrate adjacent said first spacers of said first gate conductors, wherein said first-type impurity implants are single and non-stepped; and

second-type impurity implants in areas of said substrate adjacent said second spacers of said second gate conductors, wherein said second-type impurity implants are single and non-stepped, wherein said first-type impurity is spaced closer to said first gate conductors than said second-type impurity is spaced from said second gate conductors.

2. (Currently Amended) The integrated circuit structure ~~in~~ according to claim 1, all the limitations of which are incorporated herein by reference, wherein said second spacers are only on said etch stop layer on said first spacers that are adjacent said second gate conductors, and said second spacers are not adjacent said first spacers that are adjacent said first gate conductors.

3-5. (Cancelled).

6. (Currently Amended) The integrated circuit structure ~~in~~ according to claim 4, all the limitations of which are incorporated herein by reference, wherein said first-type impurity and said second-type impurity comprises source/drain impurities.

7. (Currently Amended) The integrated circuit structure ~~in~~ according to claim 1, all the limitations of which are incorporated herein by reference, wherein said first-type transistors comprise n-type field effect transistors (NFETs) and said second-type transistors comprise p-type field effect transistors (PFETs).

8. (Currently Amended) An integrated circuit structure comprising:

a substrate;

first-type transistors on said substrate, wherein said first-type transistors comprise first gate conductors and first spacers adjacent said first gate conductors;

second-type transistors on said substrate, wherein said second-type transistors comprise second gate conductors, said first spacers adjacent said second gate conductors, an etch stop layer on said first spacers, and second spacers on said etch stop layer, wherein said etch stop layer is only on said first spacers that are adjacent said second gate conductors and said etch stop layer is not on said first spacers that are adjacent said first gate conductors;

an oxide layer, wherein said oxide layer is on said first gate conductors and said second gate conductors, wherein said first spacers are on said oxide layer, and wherein said etch stop layer is between bottom surfaces of said second spacers and said oxide layer;

first-type impurity implants in areas of said substrate completely outside of said first spacers of said first gate conductors;

second-type impurity implants in areas of said substrate completely outside of said second spacers of said second gate conductors;

first silicide regions proximate said first spacers of said first-type transistors; and second silicide regions proximate said second spacers of said second-type transistors, wherein said second silicide regions are farther from said second gate conductors than said first silicide regions are from said first gate conductors.

9. (Currently Amended) The integrated circuit structure ~~in~~ according to claim 8, all the limitations of which are incorporated herein by reference, wherein said second spacers are only

proximate said first spacers that are adjacent said second gate conductors and said second spacers are not proximate said first spacers that are adjacent said first gate conductors.

10-11. (Cancelled).

12. (Currently Amended) The integrated circuit structure ~~in~~ according to claim 8, all the limitations of which are incorporated herein by reference, wherein said first-type impurity is spaced closer to said first gate conductors than said second-type impurity is spaced from said second gate conductors.

13. (Currently Amended) The integrated circuit structure ~~in~~ according to claim 8, all the limitations of which are incorporated herein by reference, wherein said first-type impurity and said second-type impurity comprises source/drain impurities.

14. (Currently Amended) The integrated circuit structure ~~in~~ according to claim 8, all the limitations of which are incorporated herein by reference, wherein said first-type transistors comprise n-type field effect transistors (NFETs) and said second-type transistors comprise p-type field effect transistors (PFETs).

15-25. (Cancelled).

26. (Currently Amended) An integrated circuit structure comprising:

a substrate;

first-type transistors on said substrate, wherein said first-type transistors comprise first gate conductors and first spacers adjacent said first gate conductors;

second-type transistors on said substrate, wherein said second-type transistors comprise second gate conductors, said first spacers adjacent said second gate conductors, an etch stop layer on said first spacers, and second spacers on said etch stop layer, wherein said etch stop layer is only on said first spacers that are adjacent said second gate conductors and said etch stop layer is not on said first spacers that are adjacent said first gate conductors, and wherein said second spacers are only proximate said first spacers that are adjacent said second gate conductors and said second spacers are not proximate said first spacers that are adjacent said first gate conductors;

an oxide layer, wherein said oxide layer is on said first gate conductors and said second gate conductors, ~~and~~ wherein said first spacers are on said oxide layer, and wherein said etch stop layer is between bottom surfaces of said second spacers and said oxide layer;

first-type impurity implants in areas of said substrate completely outside of said first spacers of said first gate conductors;

second-type impurity implants in areas of said substrate completely outside of said second spacers of said second gate conductors;

first silicide regions proximate said first spacers of said first-type transistors; and second silicide regions proximate said second spacers of said second-type transistors, wherein said second silicide regions are farther from said second gate conductors than said first silicide regions are from said first gate conductors.

27. (Currently Amended) The integrated circuit structure ~~in accordance to~~ claim 26, all the limitations of which are incorporated herein by reference, wherein said first-type impurity is spaced closer to said first gate conductors than said second-type impurity is spaced from said second gate conductors.

28. (Currently Amended) The integrated circuit structure ~~in accordance to~~ claim 26, all the limitations of which are incorporated herein by reference, wherein said first-type impurity and said second-type impurity comprises source/drain impurities.

29. (Currently Amended) The integrated circuit structure ~~in accordance to~~ claim 26, all the limitations of which are incorporated herein by reference, wherein said first-type transistors comprise n-type field effect transistors (NFETs) and said second-type transistors comprise p-type field effect transistors (PFETs).

30. (Currently Amended) The integrated circuit structure ~~in accordance to~~ claim 1, all the limitations of which are incorporated herein by reference, further comprising an oxide layer, wherein said oxide layer is on said first gate conductors and said second gate conductors, and wherein said first spacers are on said oxide layer.

31. (Currently Amended) The integrated circuit structure ~~in accordance to~~ claim 8, all the limitations of which are incorporated herein by reference, further comprising an oxide layer,

wherein said oxide layer is on said first gate conductors and said second gate conductors, and wherein said first spacers are on said oxide layer.

32. (Currently Amended) The integrated circuit structure ~~in accordance to~~ claim 1, all the limitations of which are incorporated herein by reference, wherein said first spacers and said second spacers each comprise nitride, and wherein said etch stop layer comprises oxide.

33. (Currently Amended) The integrated circuit structure ~~in accordance to~~ claim 8, all the limitations of which are incorporated herein by reference, wherein said first spacers and said second spacers each comprise nitride, and wherein said etch stop layer comprises oxide.

34. (Currently Amended) The integrated circuit structure ~~in accordance to~~ claim 26, all the limitations of which are incorporated herein by reference, wherein said first spacers and said second spacers each comprise nitride, and wherein said etch stop layer comprises oxide.

35. (New) The integrated circuit structure according to claim 8, all the limitations of which are incorporated herein by reference, wherein said first-type impurity implants are single and non-stepped, and wherein said second-type impurity implants are single and non-stepped.

36. (New) The integrated circuit structure according to claim 26, all the limitations of which are incorporated herein by reference, wherein said first-type impurity implants are single and non-stepped, and wherein said second-type impurity implants are single and non-stepped.